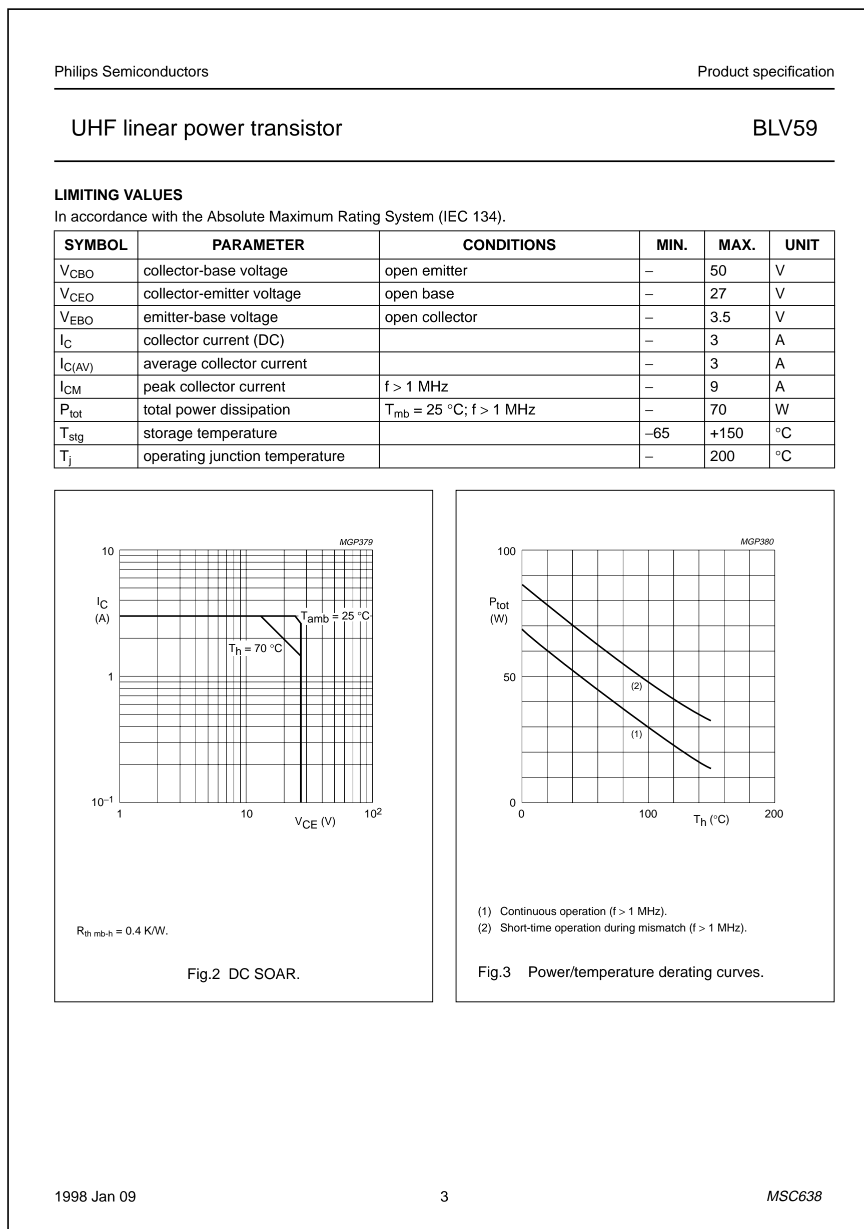
2 RF POWER TRANSISTOR CHARACTERISTICS

This section describes how to interpret and use the data published by Philips Semiconductors on its transmitting transistors.

2.1 Bipolar devices

2.1.1 Limiting values (Ratings)

As an example, consider the published data (Fig. 2-1) for the BLV59, a 30 W transistor intended for operation at up to 860 MHz from a supply voltage of 25 V, and used mainly in class-AB linear operation in TV transmitters.



Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C	collector current (DC)		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
I_{CM}	peak collector current	f > 1 MHz	–	9	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; f > 1 MHz	–	70	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

$R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.2 DC SOAR.

(1) Continuous operation (f > 1 MHz).
(2) Short-time operation during mismatch (f > 1 MHz).

Fig.3 Power/temperature derating curves.

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Fig.2-1 Part of the BLV59 data sheet showing how device *ratings* are specified.

2.1.1.1 DEFINITIONS

V_{CBO} *The maximum collector-base voltage with open emitter,* which must never be exceeded in normal operation. If this voltage is exceeded slightly, the transistor will probably not be damaged immediately. However, it will certainly produce a lot of wideband noise if the peaks of the RF voltage reach the avalanche breakdown voltage.

For some transistors, V_{CES}, the maximum collector-emitter voltage with a short circuit between base and emitter is specified. V_{CES} is almost equal to V_{CBO}.

V_{CEO} *The maximum collector-emitter voltage with open base.* The supply voltage must always be lower than this voltage otherwise the base current becomes negative. And, as there is always some DC resistance between base and emitter, this can lead to reverse second breakdown.

For some transistors, V_{CER}, the maximum collector-emitter voltage with a small resistor e.g. 10 Ω, between base and emitter is specified. V_{CER} is slightly lower than V_{CBO} and V_{CES}. With higher resistances, this voltage can approach V_{CEO}.

The relation between the different collector breakdown voltages is illustrated in Fig.2-2.

V_{EBO} *The maximum emitter-base voltage with open collector.* When the transistor is used in class-C, the average base-emitter voltage is negative, and V_{EBO} can easily be exceeded. Life tests performed under such conditions have shown that parameters such as h_{FE} and leakage currents can deteriorate. Philips Semiconductors therefore does not advise class-C operation of bipolar transistors except when the negative base-emitter bias voltage is a few tenths of a volt.

I_C *The maximum collector DC current.* This is specified to protect the emitter bonding wires and the die metallization.

I_{CM} *The maximum instantaneous value of the collector current.* Characteristics such as h_{FE} and f_T deteriorate rapidly above this value, making operation at higher levels impractical.

P_{tot} *The maximum RF dissipation at a mounting base temperature of 25 °C.* This is given only to enable different devices to be compared. In practice, the mounting base temperature will always be higher than 25 °C.

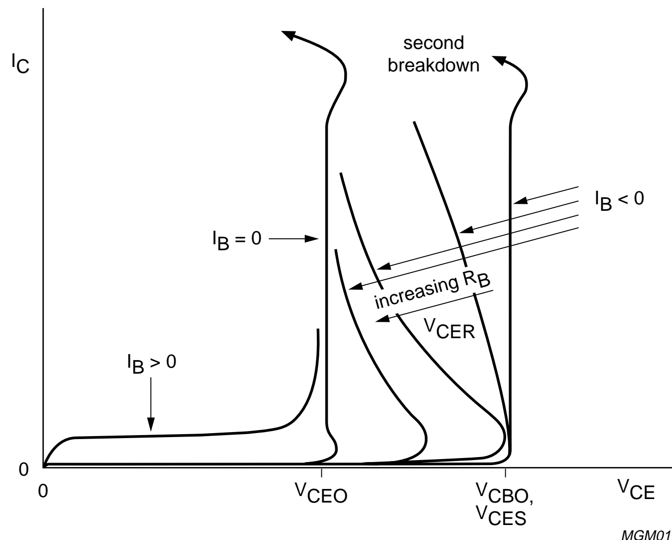


Fig.2-2 Definition of breakdown voltages.

T_{stg} *The maximum ($T_{stg\ max}$) and minimum ($T_{stg\ min}$) temperatures at which a device may be stored when not in operation.* These limits maximize storage life.

T_j *The maximum junction temperature in operation.* This is 200 °C for most silicon devices. Exceeding this value for long periods will shorten transistor life.

DC SOAR

The DC Safe Operating ARea.
This is a graph showing the maximum allowable DC collector current versus the collector-emitter DC voltage at a specified mounting base (and/or heatsink) temperature. This information is essential if a device is used in class-A. Note that the thermal resistance in DC operation is often higher (i.e. worse) than the resistance in RF operation. However, for a well-designed device, i.e. one with a built-in emitter resistance of sufficiently high value, the differences between the DC and RF SOAR are small.

Some transistors designed specifically for class-B operation have smaller built-in emitter resistances, so the allowable DC dissipation at high collector voltages is reduced to prevent forward second breakdown at these voltages. Figure 2-3 gives an example of such a DC SOAR.

Power/temperature derating curves versus heatsink temperature.
These curves give the maximum allowable RF dissipation under different conditions. A transistor's thermal resistance is not constant because the thermal resistivities of silicon, beryllia and aluminium nitride are temperature dependent, all increasing with temperature. Therefore, the thermal resistance of the transistor depends on the heatsink or mounting-base temperature and on the power dissipation.

The curve given for continuous operation (Curve I) is based on a junction temperature of 200 °C. The other curve (Curve II) is for short-term operation under mismatch conditions and is based on a maximum junction temperature of 270 to 280 °C. Clearly, the latter sort of operation reduces transistor life and should be restricted as much as possible.

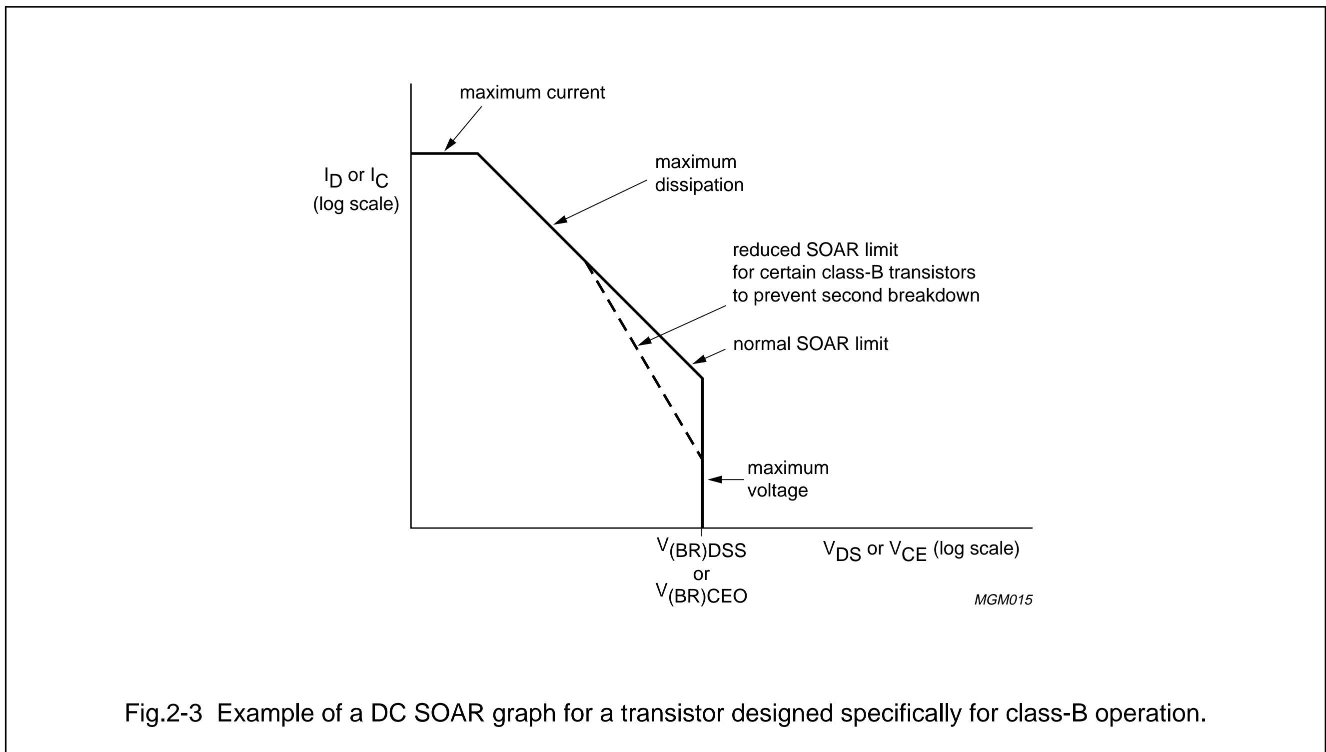


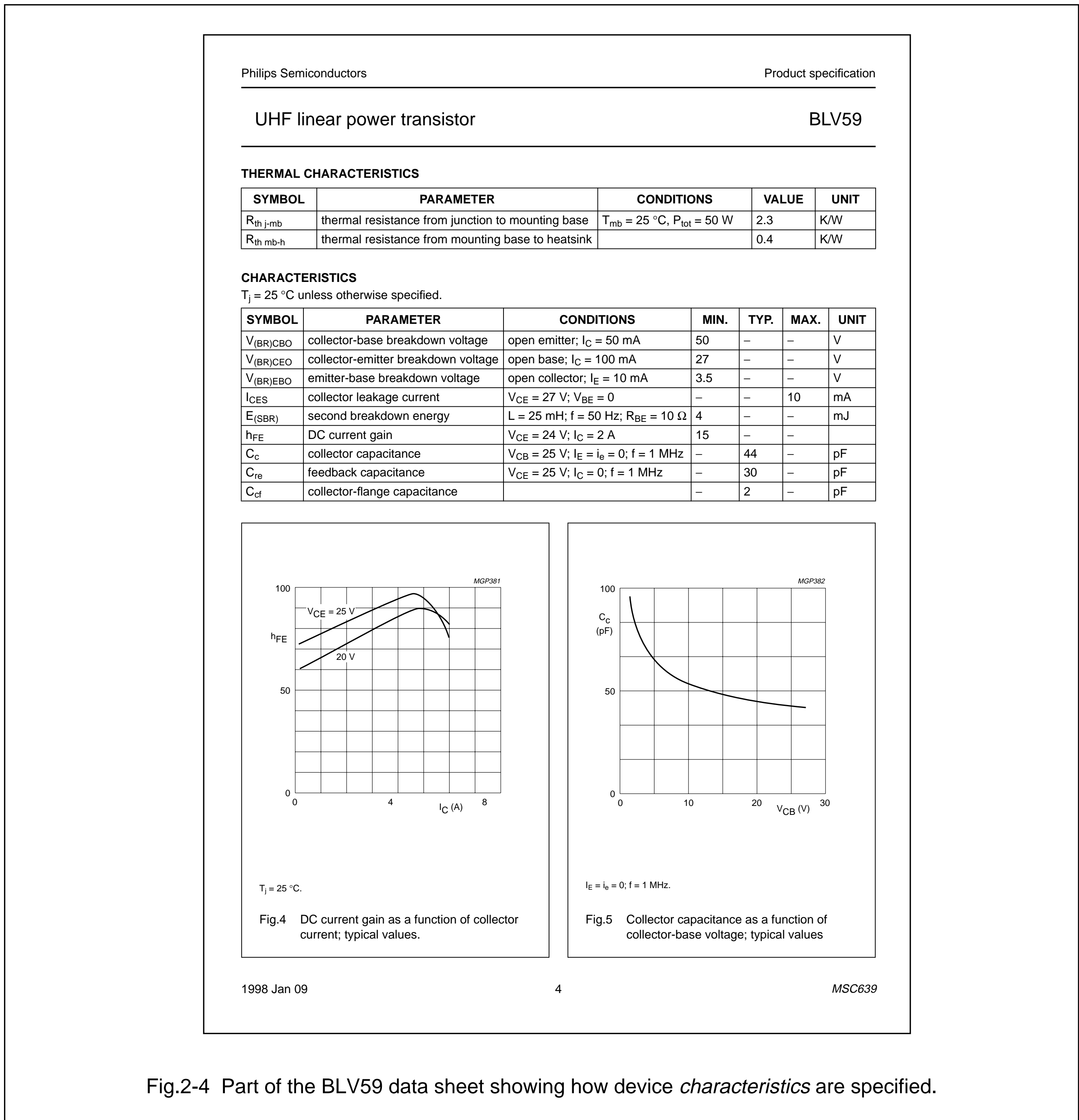
Fig.2-3 Example of a DC SOAR graph for a transistor designed specifically for class-B operation.

2.1.2 Characteristics

The BLV59 data sheet will again be used to illustrate how the main characteristics are presented in (see Fig.2-4)

2.1.2.1 THERMAL CHARACTERISTICS

Two thermal resistance values are given: from junction to mounting base, and from mounting base to heatsink. The former value is obtained from a well-defined, reproducible measurement taken under specified conditions and is guaranteed.



Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C, P_{tot} = 50 W	2.3	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 50 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 100 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	3.5	–	–	V
I_{CES}	collector leakage current	V_{CE} = 27 V; V_{BE} = 0	–	–	10	mA
$E_{(SBR)}$	second breakdown energy	L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	4	–	–	mJ
h_{FE}	DC current gain	V_{CE} = 24 V; I_C = 2 A	15	–	–	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	44	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 0; f = 1 MHz	–	30	–	pF
C_{cf}	collector-flange capacitance		–	2	–	pF

Fig.4 DC current gain as a function of collector current; typical values.

Fig.5 Collector capacitance as a function of collector-base voltage; typical values

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Fig.2-4 Part of the BLV59 data sheet showing how device *characteristics* are specified.

2.1.2.2 OTHER CHARACTERISTICS

Every transistor is subjected to a series of DC measurements to guarantee performance to specification. These measurements include the breakdown voltages mentioned earlier which are tested at specified currents, and the collector leakage current, in this example, I_{CES}, specified at a collector voltage of about half the breakdown voltage. Sometimes, other leakage currents such as I_{CEO} and I_{EBO} are specified.

h_{FE} *The DC current gain*
This is the ratio of collector and base current at specified V_{CE} and I_C. A minimum value is always given; a maximum sometimes. Matched pairs of some transistor types are available for push-pull operation.

$E_{(SBR)}$ *The (reverse) second breakdown energy*
This is measured with a coil of 25 mH in the collector lead of the transistor. First, the collector current is adjusted such that:

$$I_C = \sqrt{\frac{2E_{(SBR)}}{L}}$$

where $E_{(SBR)}$ is the specified second breakdown energy.

The current is then suddenly interrupted, causing the collector voltage to rise to the avalanche voltage and to stay there until all the energy of the coil ($LI_C{}^2/2$) is dissipated by the transistor. If the collector voltage falls before a pre-set time that represents ideal transistor behaviour, the device is deemed unable to withstand the specified energy and fails the test.

A transistor's performance in the $E_{(SBR)}$ test gives a good indication of its RF mismatch performance. Moreover, since this test can be performed much quicker than a mismatch test and has no effect on transistor life, 100% testing of $E_{(SBR)}$ is used in production instead of mismatch-testing. Samples from production are of course subjected to real mismatch testing (see Section 2.1.3.3, Ruggedness) to establish quality levels.

Several other characteristics (typical values) such as capacitances and sometimes f_T and $V_{CE\,sat}$ are given:

C_c *The total collector or output capacitance.* This is the sum of C_{cb} and C_{ce} measured at 1 MHz.

C_{re} *The feedback capacitance, i.e. C_{cb}, also measured at 1 MHz.* Both capacitances are measured at the standard supply voltage for each transistor type.

f_T *The transition frequency.* This is the frequency at which the RF value of the common-emitter current gain, h_{fe}, has fallen to one, see Fig.2-5, and is a useful performance indicator when comparing transistors. It is obtained in one measurement taken with the transistor output short-circuited. Above a certain frequency, the RF current gain, h_{fe} begins to fall off at 6 dB/octave. The measuring frequency, f_m, is chosen well above this frequency and then:
$f_T = h_{fe}f_m$.

Note: no f_T information is published for the BLV59, because this transistor has a built-in matching capacitor at its input which would make the measurement meaningless.

$V_{CE\,sat}$ *The collector-emitter saturation voltage* gives an impression of the total resistance in the collector-emitter circuit. It is measured at an I_C/I_B ratio less than the specified minimum h_{FE} to ensure the transistor is saturated.

Finally, some graphs such as h_{FE} versus I_C, C_c versus V_{CB}, and in some cases f_T versus I_C are given.

All characteristics are published at T_j = 25 °C and (with the exception of the capacitances) are obtained from pulsed measurements using pulses of short duration compared to the thermal time constant of the die.

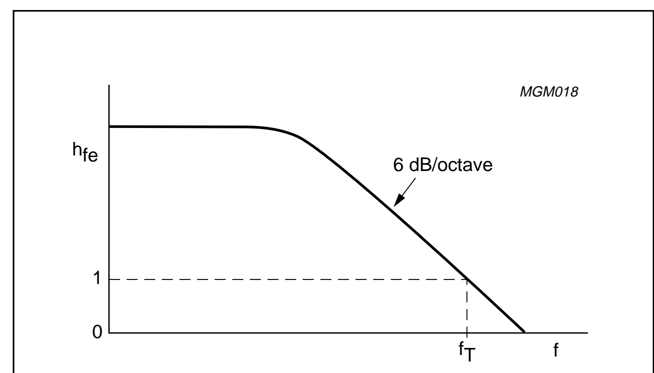
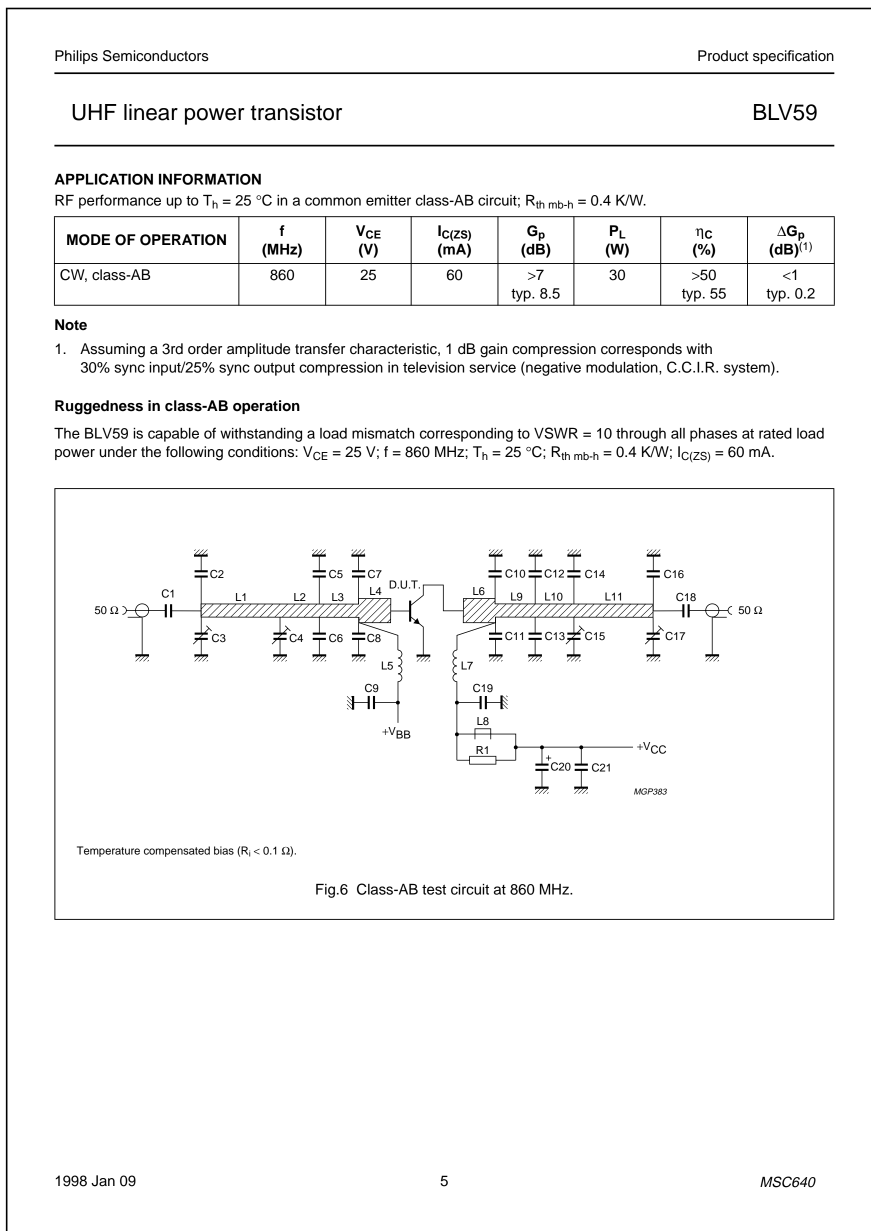


Fig.2-5 RF current gain, h_{fe} as a function of frequency. f_T is the transition frequency.

2.1.3 Application information

For each transistor type, a narrow-band test circuit is designed for the highest frequency of operation. The circuit is aligned for maximum power transfer and minimum input reflection. Important parameters such as power gain and collector efficiency (see Sections 2.1.3.1 and 2.1.3.2) are measured for each transistor from production.

To assist circuit designers, Philips Semiconductors publishes the circuit diagram and board lay-out of these test circuits (and the measured performance) in its data sheets, see Figs 2-6 and 2-7.



Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

APPLICATION INFORMATION

RF performance up to T_h = 25 °C in a common emitter class-AB circuit; $R_{th\ mb-h}$ = 0.4 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (mA)	G_p (dB)	P_L (W)	η_C (%)	ΔG_p (dB)(1)
CW, class-AB	860	25	60	>7 typ. 8.5	30	>50 typ. 55	<1 typ. 0.2

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

Ruggedness in class-AB operation

The BLV59 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases at rated load power under the following conditions: V_{CE} = 25 V; f = 860 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA.

Temperature compensated bias (R_i < 0.1 Ω).

Fig.6 Class-AB test circuit at 860 MHz.

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Fig.2-6 Part of the BLV59 data sheet showing the Class-AB test circuit for the BLV59 at f = 860 MHz. Fig.2-7 shows the board and component layout. Though omitted here, component values, descriptions and manufacturers as well as board specifications and assembly instructions are given in the data sheets for each test circuit.

2.1.3.1 *POWER GAIN*

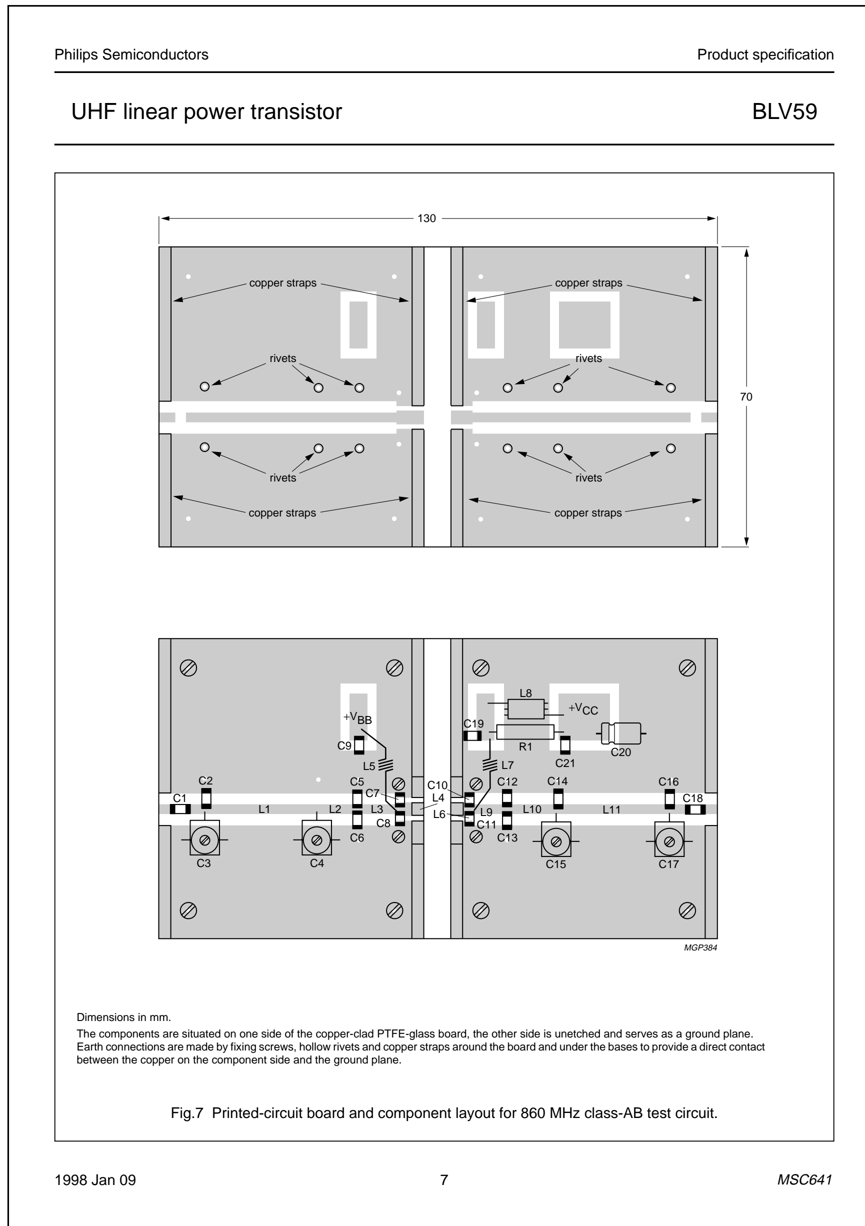
The power gain is defined as:

$$G_P = 10 \log\left(\frac{P_L}{P_S}\right) \text{ dB}$$

where:

P_L is the output power in the 50 Ω load

P_S is the forward power delivered by the 50 Ω source.



Philips Semiconductors Product specification

UHF linear power transistor BLV59

Dimensions in mm.
The components are situated on one side of the copper-clad PTFE-glass board, the other side is unetched and serves as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

Fig.7 Printed-circuit board and component layout for 860 MHz class-AB test circuit.

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Fig.2-7 Board and component layout of the circuit shown in Fig.2-6.

2.1.3.2 COLLECTOR EFFICIENCY

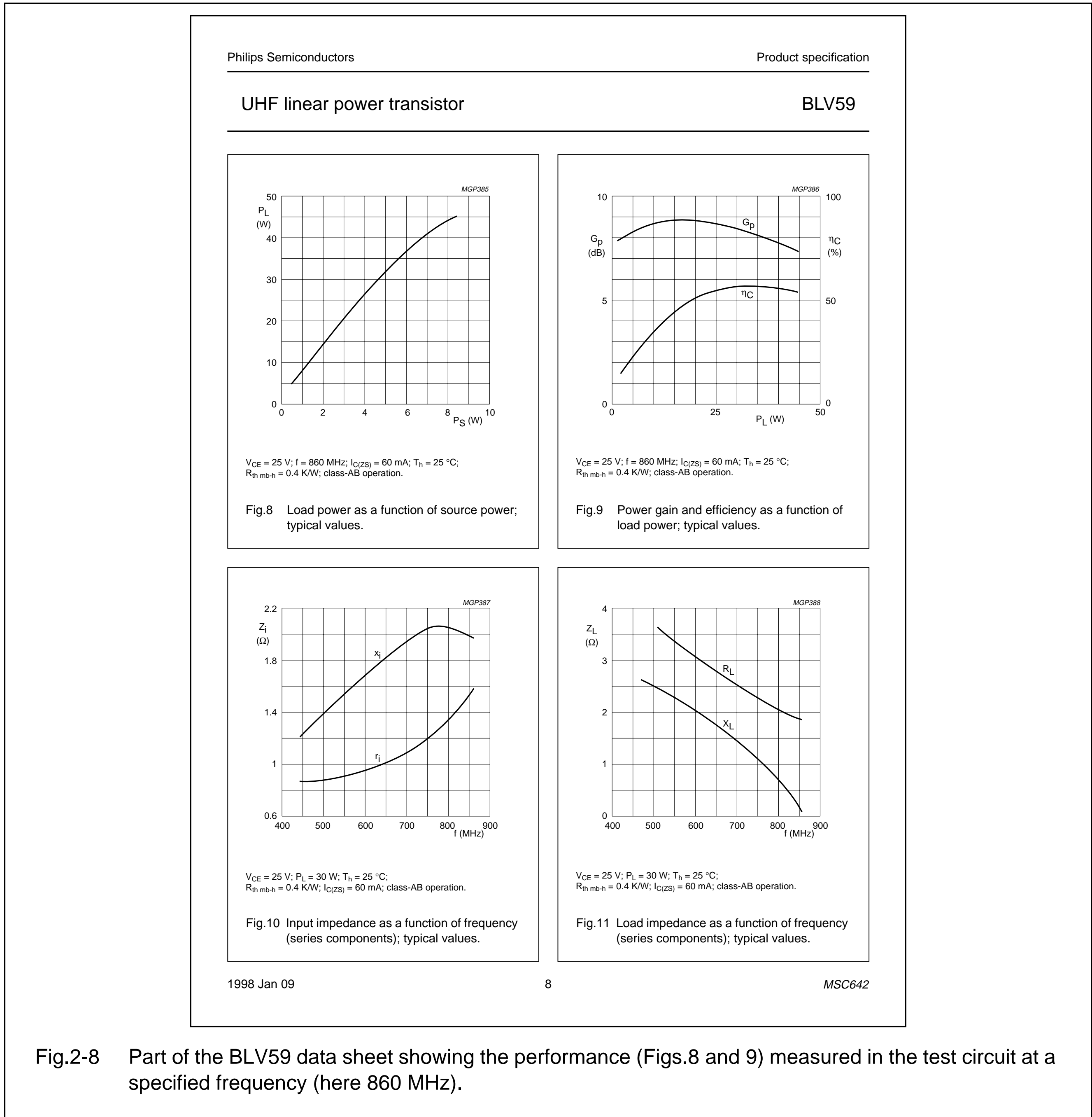
The collector efficiency is defined as:

$$\eta_c = \frac{P_L}{V_{CE} I_C} \times 100\%$$

where V_{CE} and I_C are the collector-emitter DC voltage and collector DC current respectively.

For the BLV59, the gain compression at maximum power (30 W) is also measured. The published values (all types) are all guaranteed.

Graphs are always given of load power versus source power and of power gain and efficiency versus load power (all typical values), see Fig.2-8.



Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; class-AB operation.

Fig.8 Load power as a function of source power; typical values.

V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; class-AB operation.

Fig.9 Power gain and efficiency as a function of load power; typical values.

V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.10 Input impedance as a function of frequency (series components); typical values.

V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.11 Load impedance as a function of frequency (series components); typical values.

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Fig.2-8 Part of the BLV59 data sheet showing the performance (Figs.8 and 9) measured in the test circuit at a specified frequency (here 860 MHz).

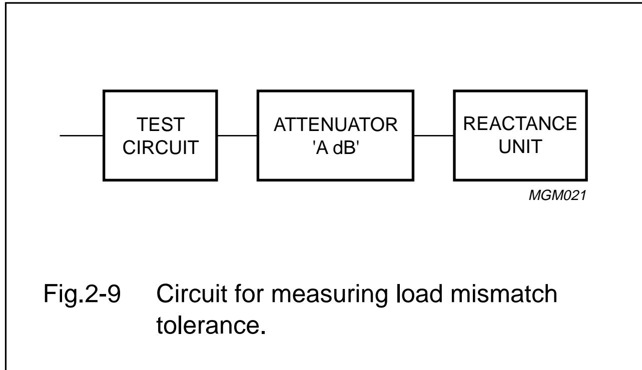


Fig.2-9 Circuit for measuring load mismatch tolerance.

2.1.3.3 RUGGEDNESS

Transistors are also tested for their ability to withstand output mismatching without any measurable degradation of performance (ruggedness). This is done by replacing the 50 Ω load impedance of the test circuit by an attenuator and reactance unit as shown in Fig.2-9.

The attenuator is dimensioned such that the VSWR required by the test is obtained according to:

$$A = 10 \log \left(\frac{s+1}{s-1} \right) \text{ dB}$$

where A is the attenuation and s is the VSWR.

The reactance unit is required to vary the phase of the reflection coefficient and has to be able to provide reactances from $-\infty$ to $+\infty$, including zero at the test frequency (usually the transistors maximum intended operating frequency). At very high frequencies, this can be done by means of a variable-length coaxial stub, variable over at least half a wavelength. At low frequencies, an LC circuit as shown in Fig.2-10 is used.

In this circuit, inductors L_1 and L_2 must be screened from each other. C_1 and C_2 is a ganged capacitor, and $C_1 = C_2$. Suitable component values are:

$X_{L1} = +j50\ \Omega$; $X_{L2} = +j200\ \Omega$

$X_{C1} = X_{C2} = -j200\ \Omega$ to $-j50\ \Omega$.

If C_1 and C_2 are set to their minimum value, the first series resonance (of L_2 and C_2) occurs, see Fig.2-11.

By increasing the capacitance of C_1 and C_2, the reactance can be varied from zero to $+\infty$ at which a parallel resonance occurs. Increasing the capacitances further changes the reactance from $-\infty$ to zero at which the second series resonance (of L_1 and C_1) occurs.

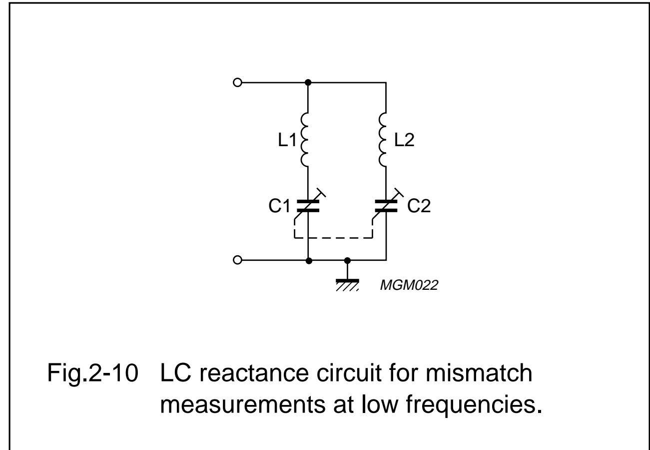


Fig.2-10 LC reactance circuit for mismatch measurements at low frequencies.

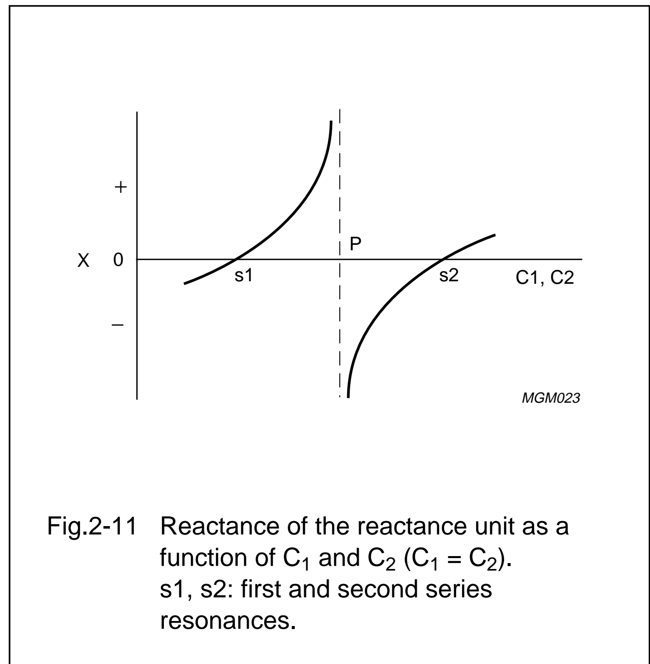
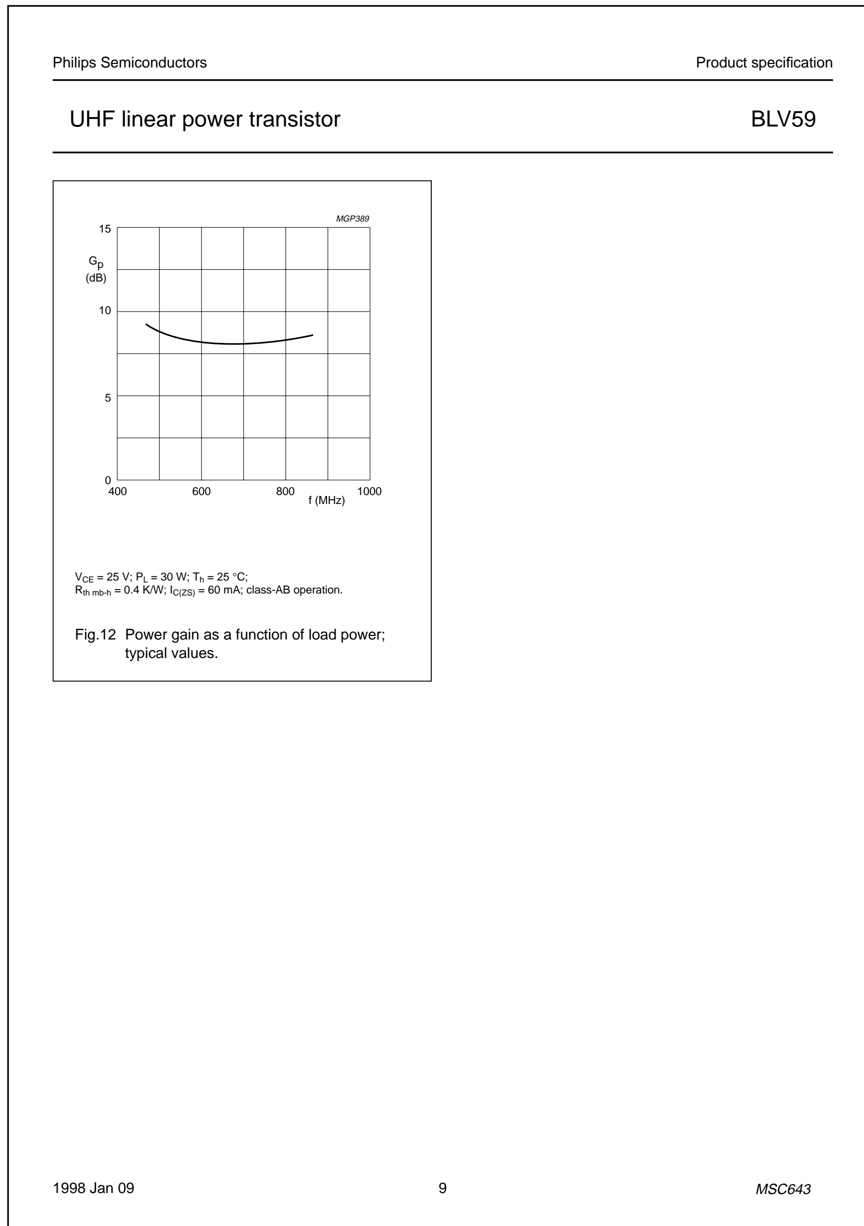


Fig.2-11 Reactance of the reactance unit as a function of C_1 and C_2 ($C_1 = C_2$). s1, s2: first and second series resonances.

2.1.3.4 GAIN AND IMPEDANCE INFORMATION

To facilitate the design of both narrowband and wideband amplifiers, graphs of input impedance, optimum load impedance and power gain over a wide range of frequencies are published in Philips' data sheets, see Fig.2-8 (Figs 10 and 11) and Fig.2-12. The published data are valid for the specified supply voltage and output power; when the conditions in your application are different, please contact Philips Semiconductors for additional information.



Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.12 Power gain as a function of load power; typical values.

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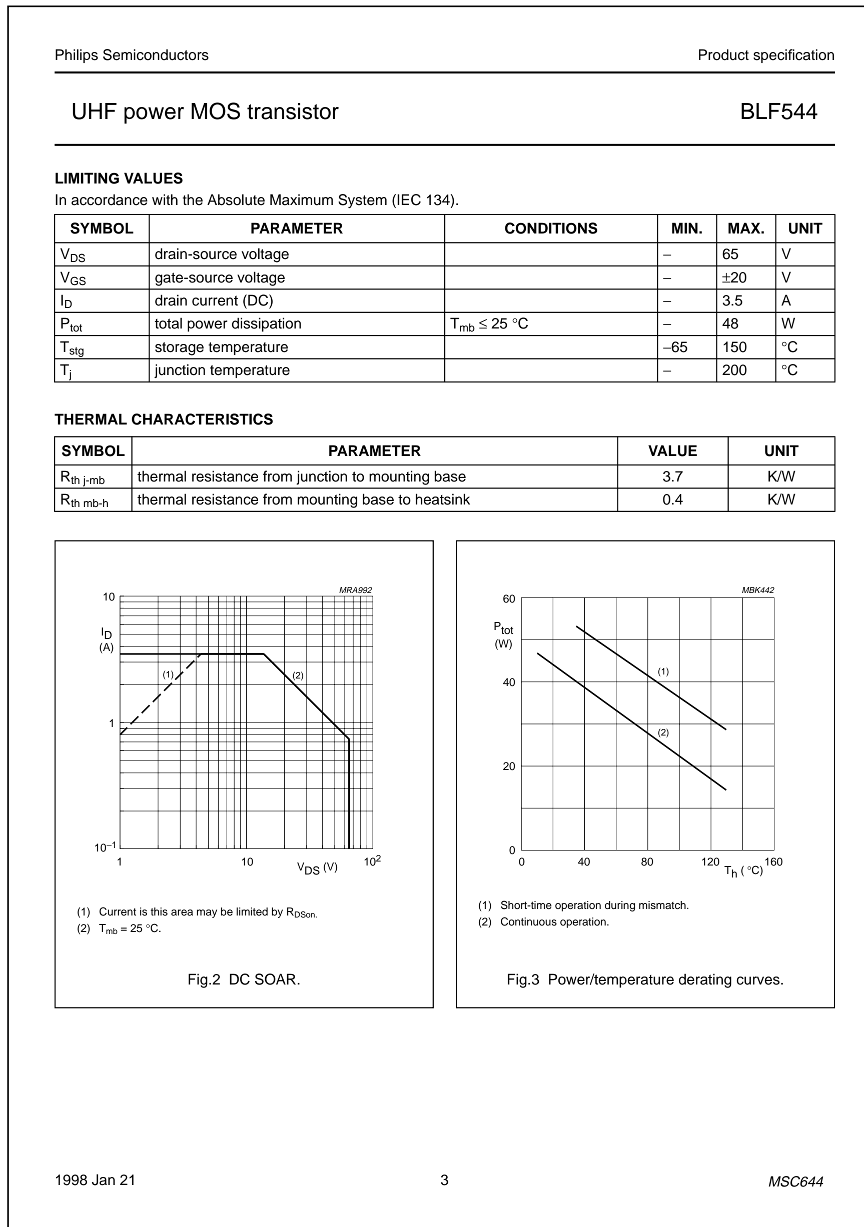
Fig.2-12 Part of the BLV59 data sheet showing additional information to assist in the design of narrow and wideband amplifiers. See also Fig.2-8.

2.2 MOS devices

2.2.1 Limiting values (Ratings)

As an example, consider the published data (Fig.2-13) for the BLF544, a silicon n-channel enhancement mode vertical DMOS transistor intended for wideband operation in the VHF/UHF range. At 500 MHz and a supply voltage of 28 V, the BLF544 has a specified output power of 20 W.



Philips Semiconductors | Product specification

UHF power MOS transistor | BLF544

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	3.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	48	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	3.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4	K/W

(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.

(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

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Fig.2-13 Part of the BLF544 data sheet showing how the device *ratings* of a MOS transistor are specified.

2.2.1.1 DEFINITIONS

Since many of the ratings of a MOS transmitting transistor are the same or very similar to those of a bipolar device, we shall discuss only the main differences, namely:

V_{DS} *Drain-source voltage*
This is equivalent to V_{CBO} for a bipolar transistor. A quantity like V_{CEO} does not exist for MOS devices.

V_{GS} *Gate-source voltage.*
This rating must be carefully adhered to. Even very small amounts of energy are able to destroy a MOS device. Static charges in particular are dangerous in this respect; ESD protection measures are essential when handling MOS transistors.

I_D *Drain current.*
This is equivalent to I_C for a bipolar transistor.

All other ratings in Fig.2-13 have the same meaning as those for bipolar transistors. Unlike bipolars however, there is no difference between the power dissipation for DC and RF operation. In the DC SOAR, there is an extra drain current limitation at low drain voltages due to $R_{DS\ (on)}$.

2.2.2 Characteristics

As the example of Fig.2-14 shows, the published data contains some well-known parameters such as breakdown voltage and leakage currents and, in addition:

$V_{GS(th)}$ *The gate voltage at which drain current starts to flow.*
As there is quite a large spread on this parameter, matched pairs of some transistor types are available for push-pull operation ($V_{GS(th)}$ matched to within <100 mV).

g_{fs} *The forward transconductance.*
This is the slope of the I_D versus V_{GS} characteristic at a specified I_D. This parameter is important for the power gain of a transistor.

$R_{DS\ (on)}$ *The total resistance in the drain-source circuit at a high, positive V_{GS}.*
$R_{DS\ (on)}$ is the main parameter that determines the drain efficiency.

C_{is} *The input capacitance when the output is short-circuited.*
This means that $C_{is} = C_{gs} + C_{gd}$ where C_{gs} and C_{gd} are the gate-source and gate-drain capacitances respectively.

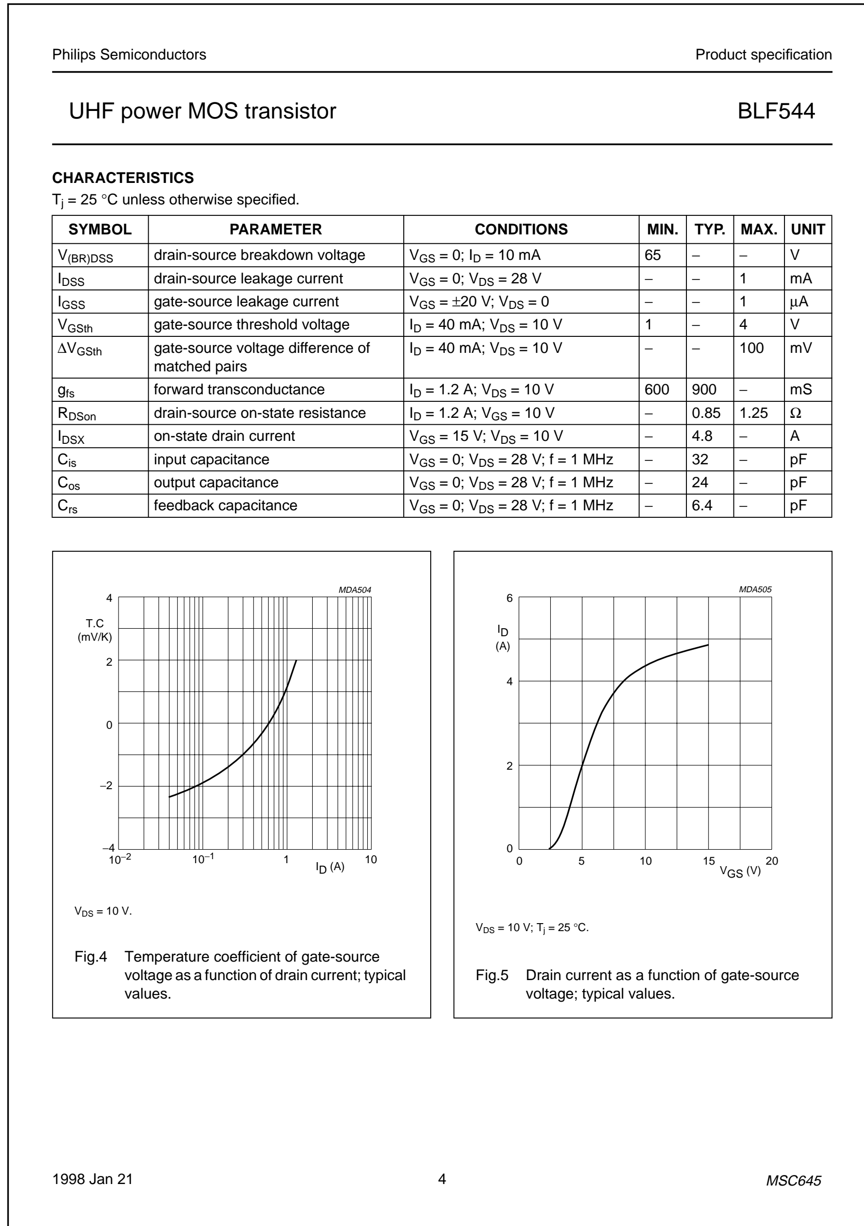
C_{os} *The output capacitance when the input is short-circuited.*
This means that $C_{os} = C_{ds} + C_{gd}$ where C_{ds} and C_{gd} are the drain-source and gate-drain capacitances respectively.

C_{rs} *The feedback capacitance.*
This is the same as C_{gd}.

I_{DSX} *The maximum drain current that the device can deliver.*
Above I_{DSX}, the transconductance is too low for practical use.

Besides the above, some graphs are given such as I_D versus V_{GS}. As this characteristic is temperature dependent, its temperature coefficient (useful when designing bias units) is given in a separate graph (see Fig.2-14).

$R_{DS(on)}$ is also dependent on junction temperature and this is shown in a graph (see Fig.2-15) Finally, the capacitances are given as functions of the drain voltage (also shown in Fig.2-15). Note, C_{is} is the sum of the gate-source capacitance and the gate-drain capacitance (equal to C_{rs}), and subtracting the latter from C_{is} shows that the gate-source capacitance is almost constant.



Philips Semiconductors — Product specification

UHF power MOS transistor — BLF544

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
ΔV_{GSth}	gate-source voltage difference of matched pairs	I_D = 40 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
R_{DSon}	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF

V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.

V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.

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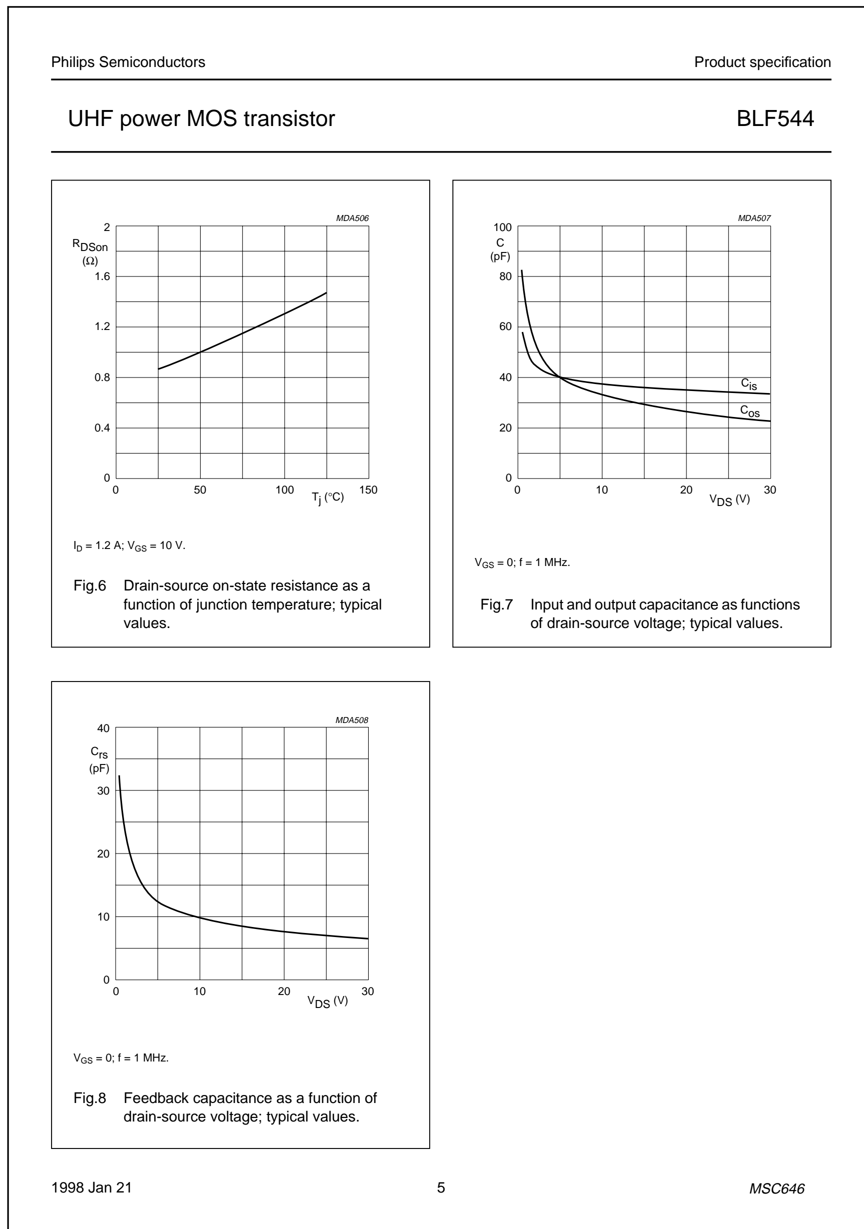
Fig.2-14 Part of the BLF544 data sheet showing how the device *characteristics* of a MOS transistor are specified.



Philips Semiconductors Product specification

UHF power MOS transistor BLF544

I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.

V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.

V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

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Fig.2-15 Part of the BLF544 data sheet showing the $R_{DS(on)}$ and capacitance graphs.

2.2.3 Application information

The published application information for MOS transistors is so similar to that for bipolar devices (see Section 2.1.3), that no further comment is needed here.

2.3 Reliability

Reliability is a measure of the ability of a device to perform its intended function over its useful lifetime under stated conditions. It is thus a measure of the quality remaining after some time and after exposure to certain operating stresses. Like other measures of quality, reliability is a probability. The failure rates of many semiconductors follow the well-known bath-tub curve, (see Fig.2-16).

2.3.1 Failure rate

The instantaneous failure rate is the sum of three components:

Early failures (infant mortalities)
These are failures of devices that initially meet the specification, but which fail due to minor latent defects exposed during the first hours of operation. Such failures are common to the fabrication processes of all semiconductor manufacturers. They can be isolated by subjecting all devices to a burn-in period.

Random failures
This is the dominant failure mode during the main period of life. Failures may occur randomly for no apparent reason. The failure rate is virtually constant during this period, the only one therefore where it is useful to specify a failure rate.

Wear-out failures
These are the increasing number of failures that occur as physical and chemical degradation processes accelerate until no working components remain.

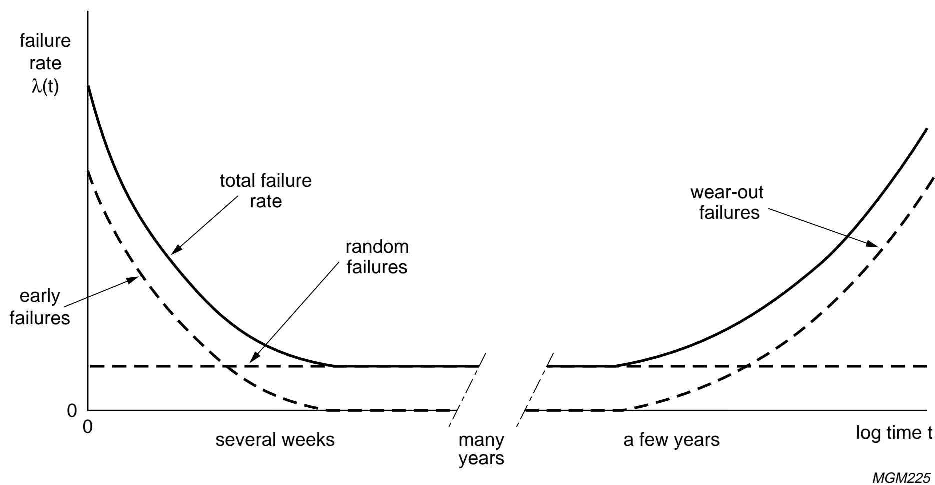

Fig.2-16 The familiar bath-tub curve of failure rate as a function of time. Note, time is given on a log scale - the period of constant failure rate is soon reached.

2.3.2 Mean-Time-To-Failure (MTTF)

During the constant failure rate period, the reliability is:
$R(t) = e^{-\lambda t}$
where:
R(t) is the probability of no failures up to time t, and
λ is the failure rate.

The MTTF is the time after which R(t) has fallen to 37% (1/e), that is, MTTF = $1/\lambda$. A device that has operated up to the MTTF therefore has a probability of survival of 0.37.

2.3.3 Median-Time-To-Failure (MTF or $t_{50\%}$)

In many instances, the cumulative failures of semiconductor devices follow a lognormal distribution. The time at which 50% of the components have failed due to wearout is called the median-time-to-failure. Note that knowledge of MTF is of little value to equipment designers; much more important, and useful, is the likely time to failure of, for example, the first 0.1% ($t_{0.1\%}$).

2.3.4 Bonding wires, metallization and barrier layers

Philips' modern range of RF transmitting transistors with gold bonding wires, gold metallization and a TiPt barrier layer (to prevent gold-silicon alloy formation) are extremely reliable especially at high junction temperatures. The use of barrier layers has enabled the potential reliability of all-gold designs to be fully exploited, and has overcome the shortcomings of all-aluminium designs such as electromigration, aluminium diffusion and thermal fatigue, and the 'purple plague' of the now-obsolete gold-aluminium hybrids.

A two-layer structure formed by depositing a platinum barrier layer on top of a titanium adhesive layer (the latter deposited on the silicon die) has proved to be highly effective at preventing alloy formation. Moreover, as the electromigration of gold is about one tenth that of aluminium, the current density in the metallization is no longer the limiting factor. And, the MTF of 'gold' transistors with barrier layers is theoretically 10^6 to 10^7 hours at a junction temperature of 200 °C. Accelerated life tests have shown that the lifetime mentioned can indeed be reached.

Published MTFs
Note, when comparing the published MTFs of different manufacturers, remember that different manufacturers base their MTFs on different failure mechanisms. Philips, for instance, includes the diffusion of gold into the die silicon, which indicates the quality of the platinum barrier layer, as a failure mechanism. Some manufacturers use electromigration measurements which can *suggest* reliability superior to that obtained using the former, more exacting, criterion.

2.3.5 Power temperature-derating

Finally, it is important to bear in mind the effect of derating. Suppose that an RF amplifier circuit has been designed such that the maximum junction temperature of the output transistor is 200 °C at maximum supply voltage and ambient temperature. This means that for most of the time, under normal operating conditions, the junction temperature will be lower, and the life of the transistor will be longer - more than double (2.4×) per 10 °C reduction in junction temperature.